

REMARKS

Claims 1-21 are pending in the application. Claims 17-21 are withdrawn from consideration as being directed to non-elected inventions. In the Office Action of July 12, 2002, the Examiner made the following disposition:

- A.) Objected to the Figures 7A and 7B.
- B.) Objected to the Title of the Invention.
- C.) Objected to the Abstract of the Disclosure.
- D.) Objected to claims 1 and 7 for informalities.
- E.) Rejected claims 1-4 and 13-14 under 35 U.S.C. §102(e) as being anticipated by *Fillion et al.*
- F.) Rejected claims 7-11 under 35 U.S.C. §102(b) as being anticipated by *Sudo et al.*
- G.) Rejected claims 5-6 and 15-16 under 35 U.S.C. §103(a) as being unpatentable over *Fillion et al.* in view of *Sharma*.
- H.) Rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over *Sudo et al.* in view of *Sharma*.

Applicants respectfully traverse the rejections and addresses the Examiner's disposition below.

A.) Objection to the Figures 7A and 7B:

In accordance with the Examiner's request, Figures 7A and 7B have been amended as indicated on the drawing sheets highlighted in red submitted with the Request for Approval of Drawing Changes submitted herewith.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

B.) Objection to the Title of the Invention:

The Title of the Invention has been amended as per the Examiner's request to overcome the objection. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE"**.

Applicants respectfully submit that the objection has been overcome and request that it be withdrawn.

C.) Objection to the Abstract of the Disclosure:

The Abstract of the Disclosure has been amended as per the Examiner's request to overcome the objection.

Applicants respectfully submit that the objection has been overcome and request that it be withdrawn.

D.) Objection to claims 1 and 7 for informalities:

Claims 1 and 7 have been amended as per the Examiner's request to overcome the objection. Specifically, in each of claims 1 and 7, the term "incrusted" has been changed to the term --encrusted--.

Applicants respectfully submit that the objection has been overcome and request that it be withdrawn.

E.) Rejection of claims 1-4 and 13-14 under 35 U.S.C. §102(e) as being anticipated by *Fillion et al.*:

Applicants respectfully disagree with the rejection.

Regarding claims 1-4:

Applicants' independent claim 1, as amended, claims a plurality of semiconductor chips mounted on an outer surface of a substrate. An insulation film is provided on the substrate, wherein a top surface and side surfaces of the plurality of semiconductor chips are encrusted in the insulation film. Wiring is provided on the insulation film, wherein the wiring is connected to the plurality of semiconductor chips through a connection hole formed on the insulation film.

This is clearly unlike *Fillion et al.*, which fails to disclose a plurality of semiconductor chips mounted on an outer surface of a substrate, or chips that are encrusted in insulation film as claimed by Applicants. Referring to *Fillion et al.* Figure 1, *Fillion et al.* discloses a plurality of chips 22, 24 mounted in cavities of a substrate 38. As described in *Fillion et al.*, the substrate 38 may be a molded substrate (Col. 3, lines 10-28) that surrounds all but a top surface of the chips or a ceramic substrate with cavities milled therein with the chips 22, 24 attached in the cavities by glue. (Col. 5, lines 51-56). In either case, *Fillion et al.*'s chips 22, 24 are mounted within the substrate, except for the top surface of the chips 22, 24. This is clearly visible in *Fillion et al.* Figure 1.

Thus, unlike Applicants' claim 1, wherein the chips are mounted on an outer surface of a substrate and encrusted by an insulating layer, *Fillion et al.* teaches encapsulating its chips within cavities of the substrate itself. For this reason alone, *Fillion et al.* fails to disclose or even suggest Applicants' claim 1.

Further, since *Fillion et al.*'s chips are encapsulated by *Fillion et al.*'s substrate with except for a top surface, *Fillion et al.* could not disclose or even suggest Applicants' claim 1, wherein a top surface and side surfaces of Applicants' chips are encrusted in an insulation film. Therefore, for this reason also, *Fillion et al.* fails to disclose or even suggest Applicants' claim 1.

Claims 2-4 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Regarding claims 13-14:

Applicants' independent claim 13 claims a plurality of semiconductor chips mounted on a substrate, wherein a circuit of a semiconductor chip among the plurality of chips is a shared circuit with another of the chips. In Applicants' specification, Applicant describes illustrative examples wherein the shared circuit can be, for example, an I/O interface for external equipment, a power supply circuit, or an electrostatic protection circuit.

This is clearly unlike *Fillion et al.*, which fails to describe that one of its chips 22, 24 is a shared circuit. *Fillion et al.* discloses two chips 22, 24 that are connected via one metallization 74. Nowhere does *Fillion et al.* disclose or even suggest that one of its chips 22, 24 is a shared chip. In fact, *Fillian et al.* fails to even address the issue. Therefore, *Fillion et al.* could not anticipate claim 13.

Claim 14 depends directly or indirectly from claim 13 and is therefore allowable for at least the same reasons that claim 13 is allowable.

Applicants respectfully submit that the rejection of claims 1-4 and 13-14 has been overcome and request that it be withdrawn.

F.) Rejection of claims 7-11 under 35 U.S.C. §102(b) as being anticipated by *Sudo et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 7 claims an insulation layer supporting a plurality of semiconductor chips, wherein a top surface and at least a portion of side surfaces of the plurality of semiconductor chips are encrusted in the insulation layer and a surface opposite the top surface of the plurality of semiconductor chips is exposed. Wiring provided on the insulation layer, wherein the wiring is connected to each semiconductor chip of the plurality of semiconductor chips through a connection hole formed on the insulation layer.

This is clearly unlike *Sudo et al.*, which fails to disclose or even suggest semiconductor chips that are encrusted in an insulation layer. *Sudo et al.* discloses chips 23 mounted on an wiring layer 20, however, nowhere does *Sudo et al.* disclose or even suggest that its chips are encrusted in its wiring layer 20. As described in *Sudo et al.*, multilevel thin film wiring layers 22 are formed on a base substrate 11. (Col. 4, lines 20-28). Then, a plurality of semiconductor chips 23 are mounted on the multilevel thin film wiring layers 20. (Col. 4, lines 29-30). Thus, unlike Applicants' claim 7, *Sudo et al.*'s chips 23 are not encrusted in an insulation layer, *Sudo et al.*'s chips are merely mounted onto *Sudo et al.*'s already existing wiring layer 20. Nowhere does *Sudo et al.* disclose or even suggest that its chips are encrusted in its wiring layer.

Therefore, *Sudo et al.* fails to disclose or even suggest Applicants' claim 7.

Claims 8-11 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

G.) Rejection of claims 5-6 and 15-16 under 35 U.S.C. §103(a) as being unpatentable over *Fillion et al.* in view of *Sharma*.

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Fillion et al.* as discussed above. *Sharma* still fails to disclose or suggest a plurality of semiconductor chips mounted on an outer surface of a substrate, or chips that are encrusted in insulation film as claimed by Applicants. Similar to *Fillion et al.*, *Sharma* discloses chips 24, 124 that are encapsulated in a substrate. Thus, *Sharma* still fails to disclose or suggest a plurality of semiconductor chips mounted on an outer surface of a substrate, or chips that are encrusted in an insulation film.

Further, contrary to the Examiner's argument, the Applicants respectfully submit that *Sharma* fails to disclose or suggest that one of its chips is a shared circuit. As stated by the Examiner, *Sharma* discloses that its chips 24, 124 are connected to slugs 50a, 50b for receiving signals or power, however, nowhere does *Sharma* disclose or suggest that one of its chips encapsulated in its substrate is a shared circuit. Applicants respectfully submit that the concept of the "shared circuit" has been read into *Sharma* by the Examiner.

Therefore, *Fillion et al.* in view of *Sharma* still fails to disclose or suggest Applicants' claims 1 and 13.

Claims 5-6 and 15-16 depend directly or indirectly from claims 1 or 13 and are therefore allowable for at least the same reasons that claims 1 and 13 are allowable.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

H.) Rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over *Sudo et al.* in view of *Sharma*.

Applicants respectfully disagree with the rejection.

Applicants' independent claim 7 is allowable over *Sudo et al.* as described above. *Sharma* still fails to disclose or suggest chips that are encrusted in insulation film as claimed by Applicants. Similar to *Fillion et al.*, *Sharma* discloses chips 24, 124 that are encapsulated in a substrate. Thus, *Sharma* still fails to disclose or suggest chips that are encrusted in insulation film, as claimed by Applicants.

Further, contrary to the Examiner's argument, the Applicants respectfully submit that *Sharma* fails to disclose or suggest that one of its chips is a shared circuit. As stated by the Examiner, *Sharma* discloses that its chips 24, 124 are connected to slugs 50a, 50b for receiving signals or power, however, nowhere does *Sharma* disclose or suggest that one of its chips encapsulated in its substrate is a shared circuit. Applicants respectfully submit that the concept of the "shared circuit" has been read into *Sharma* by the Examiner.

Therefore, *Sudo et al.* in view of *Sharma* still fails to disclose or suggest Applicants' claim 12.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-16 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title of the Invention:

Please replace the Title of the Invention with the following replacement Title of the Invention:

--SEMICONDUCTOR DEVICE HAVING A PLURALITY OF ENCRUSTED SEMICONDUCTOR CHIPS [AND PROCESS FOR FABRICATING THE SAME]--

In the Abstract of the Disclosure:

Please replace the Abstract of the Disclosure with the following replacement Abstract of the Disclosure:

--A semiconductor device of MCM type allowing high-density assembly and a process of fabricating the same is provided. There are provided semiconductor chips mounted on a supporting substrate and incrustated in an insulation film on the supporting substrate and wiring formed in the insulation film so as to connect to each semiconductor chip through connection holes provided in the insulation film. Then, an interlayer dielectric covers such wiring that is connected to an upper layer wiring, through connection holes provided in such interlayer dielectric. In addition, an upper layer insulation film covers the upper layer wiring, and an electrode, connected to such upper layer wiring through another connection hole, is provided on such upper layer insulation film.

[There are provided semiconductor chips mounted on a supporting substrate and incrustated in an insulation film on the supporting substrate and wiring formed in the insulation film so as to connect to each semiconductor chip through connection holes provided in the insulation film. Then, an interlayer dielectric covers such wiring that is connected to an upper layer wiring, through connection holes provided in such interlayer dielectric.

In addition, an upper layer insulation film covers the upper layer wiring, and an electrode, connected to such upper layer wiring through another connection hole, is provided on such upper layer insulation film.]--

In the Claims:

Please amend claims 1 and 7 as follows:

1. (Amended) A semiconductor device, comprising:
a plurality of semiconductor chips mounted on [a] an outer surface of a substrate;
an insulation film provided on said substrate, wherein a top surface and side surfaces of
said plurality of semiconductor chips are [incrusted] encrusted in said insulation film; and
wiring provided on said insulation film, wherein said wiring is connected to said plurality
of semiconductor chips through a connection hole formed on said insulation film.

7. (Amended) A semiconductor device, comprising:
a plurality of semiconductor chips;
an insulation layer supporting said plurality of semiconductor chips, wherein a top surface
and at least a portion of side surfaces of said plurality of semiconductor chips [is incrusted] are
encrusted in said insulation layer and [another] a surface opposite said top surface of said
plurality of semiconductor chips [are] is exposed; and
wiring provided on said insulation layer, wherein said wiring is connected to each
semiconductor chip of said plurality of semiconductor chips through a connection hole formed
on said insulation layer.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Asst. Commissioner for Patents, Washington, D.C. 20231 on August 30, 2002.

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